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APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: SELECTIVE BANK REFRESH

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SELECTIVE BANK REFRESH

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to the field of memory systems, and in particular memory systems that employ a refresh operation.

Discussion of Related Art

[0002] It is well known in the art that various types of personal computers, such as desktop computers and battery-operated notebook computers, include a central processing unit (CPU) and a main memory to which the central processing unit accesses. The central processing unit executes programs loaded on the main memory, and sequentially writes the results obtained by program execution into work areas in banks of the main memory so that the computer processing is performed.

[0003] The main memory is composed of a random access memory (RAM), such as SRAM (static RAM) and DRAM (dynamic RAM). For the main memory, DRAM is generally used because DRAM has a simple cell structure and is cheaper. Accordingly, the discussion to follow will concentrate on known DRAM memory systems.

[0004] DRAM memory cells in the main memory are arranged as a matrix. In order to address memory cells individually, first, an Activate Command is issued with a row address, and then, read or write commands are issued with the column address. In the DRAM memory cells, data are stored as electric charges on a capacitor. Thus, when data are written to the memory cells and are left for an extended period of time, the charges leak from the capacitor

and the stored data are lost. To prevent such data loss, the written data needs to be refreshed/rewritten at predetermined time intervals.

[0005] Known refresh operations include accessing a specific memory cell row to refresh all of the cells along that row. In order to refresh all of the row addresses, a refresh address counter is required that designates refresh addresses sequentially. In addition, the known refresh operations provide either a refresh cycle or issue a refresh request at a predetermined period of time.

[0006] One known method to refresh the memory contents is to serially access all rows with an activate – precharge command-sequence. For this method, a refresh address counter designates refresh row addresses that must be provided from outside the memory.

[0007] A second known refresh operation is generally known as autorefresh where a refresh request is supplied to the memory by sending an Autorefresh command. The refresh addresses are generated by an address counter within the DRAM such that no external address counter is required.

[0008] A third known refresh operation is self-refresh, which allows the data in the DRAM to be refreshed even while the rest of the system is powered down. During self-refresh an internal timing circuit and an internal address counter generate the refresh operations for all rows in time intervals sufficiently short to keep the stored data intact. This allows for very low power consumption since the time-intervals between refreshes can be optimized and all other circuits can be powered down.

[0009] FIG. 1 is a schematic diagram illustrating the arrangement of a known computer system 100 that has both the normal refresh function and the self-refresh function. A DRAM device 102, including a DRAM array_103, and a memory controller unit 104 are connected to each other by a bus 106 and an I/O device 108. Outside the DRAM device 102 are provided a normal refresh circuit 110, which forms a part of the memory controller unit 104 that performs a refresh operation while the memory controller unit 104 is accessing the memory, and a global clock 112. Inside the DRAM device 102 are provided a self-refresh circuit 114 that performs a relatively slow refresh operation, and an internal timing generator 116 that supplies a relatively long interval signal to the self-refresh circuit 114. In addition, a switch 118 is provided to select either the normal refresh circuit 110 or the self-refresh circuit 114 for refreshing the DRAM device 102.

[0010] Should the switch 118 select the self-refresh circuit 114, then as previously described the known method of self-refresh is used to refresh all banks within the DRAM array 103 at the same time or to program externally which banks or parts of banks are refreshed. This can lead to situations where banks are refreshed which do not need to be refreshed since their contents are irrelevant. This is assumed to be the case if data has never been written into a bank. Due to the fact that each refresh sequence of activating and precharging a row-address costs energy, such unnecessary refresh operations cause unnecessary power consumption.

SUMMARY OF THE INVENTION

[0011] A first aspect of the present invention regards a memory control system which includes a memory controller and a memory device connected to the memory controller via a command bus, wherein command signals are directed from the memory controller to the memory device. The memory device includes several memory banks, a bank refresh indicator register, and a command decoder that is connected to the bank refresh indicator and receives the command signals and controls the contents of the bank refresh indicator register. A refresh circuit connected to the several memory banks and the bank refresh indicator register, wherein the refresh circuit avoids unnecessary power consumption for refreshing particular ones of the several memory banks with irrelevant contents.

[0012] A second aspect of the present invention regards a method of refreshing several memory banks of a memory device that receives command signals from a memory controller. The method includes monitoring command signals received by the memory device and refreshing the several memory banks based on the monitored command signals so as to avoid unnecessary power consumption for refreshing particular ones of the several memory banks with irrelevant contents.

[0013] The above aspect of the present invention provides the advantage of reducing power during self-refreshing of a memory system.

[0014] The present invention, together with attendant objects and advantages, will be best understood with reference to the detailed description below in connection with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 schematically shows an embodiment of a known memory device that includes normal and self-refresh circuits;

[0016] FIG. 2 schematically shows a first embodiment of a memory system in accordance with the present invention; and

[0017] FIG. 3 shows a flow chart of an embodiment of a refresh process in accordance with the present invention to be used with the memory system of FIG. 2.

DETAILED DESCRIPTION OF THE INVENTION

[0018] The present invention is best understood by a review of the embodiments and modes of operation represented by FIGS. 2 and 3. As shown in FIG. 2, a memory system 200 includes a memory controller 202 and a memory device 204. The memory controller 202 executes memory accesses (including both read accesses and write accesses) of the memory device 204 in response to memory access requests issued by a central processing unit (not illustrated).

[0019] The memory controller 202 and the memory device 204 are connected together by a command bus 205 of command signals, an address bus 207 of address signals, and a data bus 209 of data signals, clock signals (not illustrated) and datastrobe signals (not illustrated).

[0020] The memory controller 202 has a normal refresh circuit 206 that performs a normal refresh operation in a manner similar to that described previously. The normal refresh circuit 206 provides a normal refresh cycle

every predetermined interval, by sending an autorefresh signal to the memory device 204 through the command bus 205.

[0021] Incorporated in the memory device 204 are a self-refresh circuit 210, a self-refresh timer 214, a command decoder 216, and a bank refresh indicator register 212. The self-refresh circuit 210 includes a refresh address counter for incrementing a row address to be refreshed at each refresh cycle, and a controller for, in response to a refresh request, controlling access to a row address such that all rows get refreshed within a given time period to avoid loss of memory contents. The address counter covers all row-addresses and restarts at the lowest row address after the highest row-address has been refreshed. The incorporated refresh circuit 210 executes either a "normal refresh" operation and a "self-refresh" operation upon receipt of a corresponding refresh request. A normal refresh operation is realized by responding to a memory autorefresh refresh request from the normal refresh circuit 206, and by accessing a designated row address.

[0022] A self-refresh operation is begun when the memory device 204 is put into self-refresh mode through the respective command sequence from the memory controller 200. In the self-refresh mode, a self-refresh request is issued to the self-refresh circuit 210 from the memory controller 200 every predetermined time period that is triggered by a self-refresh timer 214. In state-of-the art memories devices, such a self-refresh circuit leads to an activate / precharge sequence for all memory banks 208 of the memory device 204 in parallel. An example of a known self-refresh circuit that can be adapted for use with the present invention is the 256Mbit-DDR-SDRAM

manufactured and sold by Infineon under the part number HYB25D256160BT-6.

[0023] As shown in FIG. 2, the memory device 204 includes a bank refresh indicator register 212 that is in communication with both a command decoder 216 and the self-refresh circuit 210. The register 212 has one bit for each memory bank 208.

[0024] The command decoder 216 monitors all write commands directed to the memory banks 208 and controls the contents of the bank refresh indicator register 212. In the discussion to follow, the bit corresponding to the ith memory bank will be denoted by B_i, wherein i = 0, 1, 2, . . . n. Each bit B_i identifies whether or not the ith memory bank has to be refreshed during a self-refresh operation. Each bit B_i can also be implemented in such a way that it identifies whether or not the ith memory bank has to be refreshed in any case of auto-refresh or self-refresh. For example, if the bit B_i is in a high state, then the ith memory bank must be refreshed. If the bit B_i is in a low state, then the ith memory bank does not need to be refreshed. A memory bank i is denoted as requiring refreshing whenever data have been written to this bank since power-up of the memory device or since the last reset of the respective bit B_i by a special command sequence.

[0025] The contents of the bank refresh indicator register 212 are all initially set to low-level during the power-up sequence of the memory device 204. Afterwards, the contents of the bank refresh indicator register 212 are controlled by the command decoder 216 of the memory device 204. Whenever a write-command is issued to the memory device 204, the

command decoder 216 decodes this write command and also decodes the bank-address to which date are written. Next, the command decoder 216 sets the respective bit B_i of the addressed bank in the bank refresh indicator register 212 to a high-level. Thus, the command decoder 216 identifies which ones of the memory banks contains data. A command sequence, usually referred to as an extended mode register set can be used to program/reset single bits or all of the bits of the bank refresh indicator register 212 to a low-level. Thus, the command sequence programs the bank refresh indicator register 212 and declares the contents of the respective memory banks 208 as relevant and without necessity to be refreshed.

[0026] The self-refresh circuit 210 monitors the contents of the bank-refresh indicator register 212 and starts the activate/precharge sequence only for those banks where the respective bit B_i of the bank-refresh indicator register 212 is set to the high-level. For those banks where the respective bit B_i is low, the self-refresh circuit 210 suppresses the refresh of wordlines of those banks. Thus, the circuit 210 avoids unnecessary power consumption for refreshing banks which are defined to not require to be refreshed by a low-level of the respective bit B_i in the bank refresh indicator register 212. The circuit 210 can be altered in such a way that it either checks the bank refresh indicator register 212 1) only in case of self-refresh mode or 2) both in self-refresh and auto-refresh mode.

[0027] As shown in FIG. 3, two parallel processes are controlling the self-refresh - and with respective implementation also autorefresh - process 300. The two processes are performed by a global control circuit that includes the

command decoder 216. The sub-process 302 controls the contents of the bank refresh indicator register 212. At power-up of the memory device (step 304), all bits B_i of the register get reset to low level (equal to logical 0) per step 306. Whenever a command is detected at the memory device 204 by the command decoder 216, the command is checked if it is an extended mode register set to the bank refresh indicator register 212 per step 308. If it is, then the bank-address given in the extended mode register set is decoded by the command decoder 216 per step 310 and the respective bit B_i of the bank refresh indicator register 212 is set or reset per step 312 to the value as given, too, in the extended mode register set. If the command is not an extended mode register set or the bit has been set/reset per step 312, the command is checked if it is a write command per step 314. In case a write command is detected, the bank-address gets decoded per step 316 and the respective bit B_i gets set to high-level (equal to logical 1) per step 318. The second parallel sub-process 320 is the refresh flow. Whenever a self-refresh or an auto-refresh is detected per step 322, the self-refresh circuit reads out the contents of the bank-refresh indicator register per step 324 prior to activating row of the banks during a refresh operation. Then, only those banks are refreshed whose respective bit B_i of the bank-refresh indicator register had a low-level (equals to a logical 0) per step 326.

[0028] Based on the above description of the process 300, the design of memory controller 200 and memory device 204 based on existing DRAM products from vendors like Samsung, Micron, Elpida and Infineon is very straightforward for any DRAM designer or general logic designer.

[0029] The foregoing description is provided to illustrate the invention, and is not to be construed as a limitation. Numerous additions, substitutions and other changes can be made to the invention without departing from its scope as set forth in the appended claims.